TRANSMITTAL FORM

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Total Number of Pages in This Submission	32

Application No.	10/028,858
Filing Date	December 19, 2001
First Named Inventor	Shivandan Kaushik
Art Unit	2112
Examiner Name	Tim T. Vo
Attorney Docket Number	42390P13163

ENCLOSURES ***(check all that apply)***

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
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- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
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- [ ] After Allowance Communication to Group
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- [x] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
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- [x] Other Enclosure(s) *(please identify below):*

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Mark C. Van Ness, Reg. No. 39,865 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	July 6, 2005

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Rachael L. Brown		
Signature		Date	July 6, 2005

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
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FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451		2451		Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($) 500.00

SUBMITTED BY Complete (if applicable)

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Signature				Date	07/06/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Shivnandan D Kaushik et al. for
Intel Corporation

Serial No.:	10/028,858	Group Art Unit:	2112
Filed:	December 19, 2001	Examiner:	VO, TIM T.

FOR: **HOT PLUG INTERFACE CONTROL METHOD AND APPARATUS**

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant (hereinafter Appellant) submits this appeal brief, thus perfecting the notice of appeal filed on May 9, 2005. The required headings and subject matter follow.

(i) Real party in interest.

This case is assigned of record to Intel Corporation, who is the real party in interest.

(ii) Related appeals and interferences.

There are no known related appeals and / or interferences.

(iii) Status of claims.

Claims 1-10, 12-14 and 16-34 are pending and stand rejected.

(iv) Status of amendments.

No amendments were filed subsequent to the final rejection.

(v) Summary of claimed subject matter.

Claim 1 relates to a method that comprises identifying one or more caching agents 230, 510 provided by a hot plug module 110 in response to the hot plug module 110 being physically coupled to the running computing device and adding the identified caching agents 230, 510 of the hot plug module 110 to a resource pool of the running computing device (See, blocks 934, 938 of FIG. 9C, paragraphs [0060] and [0062]). The method further comprises enabling a communication interface 214 of the hot plug module 110 to establish a communication link with a running computer system (See, blocks 1001-1002 of FIG. 9H, paragraphs [0084]-[0085]).

Claim 8 relates to a method that comprises identifying memory 240 of the hot plug module 110 in response to the hot plug module 110 being physically coupled to the running computing device. (See, FIGS. 2, 4, 9C, block 936, paragraph [0061]). The method further comprises adding the identified memory 240 of the hot plug module 110 to a memory pool of the running computing device (See, block 936 of FIG. 9C, paragraph [0061]).

Claim 16 relates to a machine readable medium (paragraph [0048]) for interrupt processing that comprises a plurality of instructions that in response to being executed

result in a computing device examining a plurality of interface control registers 706 associated with a plurality of communication interfaces 628 for communicating with a plurality of hot plug modules 110 having caching agents 230, 510 in response to a hot plug interrupt. The machine readable medium further comprises instructions that result in the computing device identifying which of a plurality of hot plug events caused the hot plug interrupt based upon the plurality of interface control registers 706. (See, e.g., FIGS. 7 and 9A, paragraphs [0041], [0049], [0058], [0066], [0069])

Claim 24 relates to a hot plug module 110 that comprises a coupler 112 for detachably coupling the hot plug module 110 to a running computing device. (FIGS. 1-5). The hot plug module 110 further comprises a communication interface 214 to establish a communication link with the running computing device via the coupler 112 in response to being enabled and to de-establish the communication link in response to being disabled. (See, block 996 of FIG. 9H, block 920 of FIG. 9B, paragraphs [0057] and [0081]). The hot plug module 110 also comprises an interface control register 706 associated with the communication interface 214 to indicate and control whether the communication interface 217 is enabled or disabled. (See, paragraph [0042]). The hot plug module 110 further comprises a processor 230 and associated memory cache 232 wherein the processor 230 programs the interface control register 706 to enable and disable the communication interface based upon whether the hot plug module 110 is ready to join the running computing device. (See, FIG. 3 and paragraphs [0042], [0057] and [0081]).

Claim 28 is related to a computing device 100 that comprises a midplane 120, 600 having a coupler 122 and a hot plug interface 626 to track a state associated with

the coupler 122. (See, FIGS. 1, 6 and 7, paragraphs [0028], [0038]). The computing device 100 may further comprise a hot plug module 110 comprising a coupler 110 to detachably couple the hot plug module 110 to the coupler 122 of the midplane 120, 600 and resources coupled to the coupler 112 of the hot plug module 110 via a hot plug interface 212 of the hot plug module 110. (See, FIGS. 1-5). The hot plug module 110 updates the state of the hot plug interface 626 of the midplane 120, 600 to indicate when the resources are ready to join the computing device 100. (See, FIG. 1-6 and 9G, paragraph [0079]). The computing device also comprises a processor 230, 636 coupled to the hot plug interface 626 of the midplane 120, 600. The processor 230, 636 adds the resources to the computing device 100 without rebooting in response to determining that the hot plug interface 626 of the midplane 120, 600 indicates the resources are ready to join (See., FIG. 9C).

Claim 31 relates to a midplane 120 that comprises a plurality of couplers 122 to detachably couple hot plug modules 110 to the midplane 120 and at least one switch 624 to interconnect the plurality of couplers 122. (See, FIG. 6). The switch 624 comprises a plurality of communication interfaces 628 to establish communication links with the hot plug modules 110 that are coupled to the plurality of couplers 122, and a plurality of interface control registers 706 to control the plurality of communication interfaces 628 (See, Figs. 1, 6 and 7, paragraphs [0028]-[0031] and [0041]).

(vi) Grounds of rejection to be reviewed on appeal

Claims 1-10, 12-14, and 16-34 stand rejected under 35 U.S.C. § 102(e), as being anticipated by US Patent No. 6,282,596 (Bealkowski). Only the rejection of claims 1-10 and 16-34 are appealed herewith. The rejection of Claims 12-14 is not appealed.

(vii) Argument.

The rejection of Claims 1-10 and 16-34 under 35 U.S.C. § 102(e), as being anticipated by US Patent No. 6,282,596 (Bealkowski) is in error and should be reversed.

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claims 1 and 5

Claims 1 and 5 require enabling a communication interface ***of the hot plug module*** to establish a communication link with a running computer system. Bealkowski appears to teach a hot-pluggable system bus for processor cards 11a-11d. However, the processor cards 11a-11d appear to have no communication interface, or at least Bealkowski appears to provide no teaching regarding enabling a communication interface of the processor cards 11a-11d which are presumably being equated with the "hot plug module" limitation of claims 1 and 5. Bealkowski discloses FET switches 82, 86 to control power supplied to the processor cards 11a-11d. Bealkowski further discloses a clock buffer to control application of clock signals to the processor cards

11a-11d. Moreover, Bealkowski discloses FET switches 80 that provide front-side isolation to maintain electrical integrity during hot-plug.

However, as clearly depicted in Bealkowski FIGS. 3A and 3B, the FET switches 80, 82, 86 and the clock buffer are all on the computer system side of the CPU connectors 14 and are not part of the processor cards 11a-11d. It appears that the Official Action is relying on these FET switches 80, 82, 86 and clock buffer for a teaching of a "communication interface". However, even if these components qualify as a communication interface, the FET switches 80, 82, 86 are not part of the processor cards 11a-11d and thus are not equivalent to "a communication interface **of a hot plug module**" as required by Appellant's claims 1 and 5.

Since Bealkowski appears to only disclose enabling components (e.g. switches 80, 82, 86) that are not part of a hot plug module, Bealkowski does not teach enabling ***a communication interface of a hot plug module*** as required by Appellant's claims 1 and 5. Appellant respectfully requests the rejection of claims 1 and 5 be reversed.

Claims 2-4

Each of claims 2-4 depends from claim 1. Accordingly, each of claims 2-4 is allowable for at least the reasons stated above in regard to claim 1. Further, each of claims 2-4 requires both a communication interface of the hot plug module and a communication interface of a running computer system. The Official Action appears to overlook this aspect of the claims 2-4 since the Official Action does not appear to clearly identify which components of Bealkowski are being relied upon for a teaching of the communication interface of the hot plug module and which components of Bealkowski

are being relied upon for a teaching of the running computing system. Appellant respectfully submits that Bealkowski does not disclose both ***a communication interface of a hot plug module*** and ***a communication interface of a running computer system*** and therefore does not anticipate the invention of Appellant's claims 2-4. Appellant respectfully requests the rejection of claims 2-4 be reversed.

Claim 6

Claim 6 depends from claim 1. Accordingly, claim 6 is allowable for at least the reasons stated above in regard to claim 1. Further, claim 6 requires adding one or more memory caching input/output hubs to an input/output pool of the running computer system. The Official Action on page 11 appears to be relying on the processor cards 11a-11d and the disclosed L2 caches of the processors for a teaching of a caching input/output hub. Appellant respectfully submits that one skilled in the art would not equate the "caching input/output hub" limitations of claim 6 with the processor cards 11a-11d of Bealkowski. The term input/output hub (I/O hub) is a well defined term in the computer architecture arts and is commonly used to refer to a component that acts like a traffic cop in directing I/O traffic to, from, and between I/O devices. An embodiment of an I/O hot plug module that comprises an I/O hub 510 is depicted in FIG. 5 and described in paragraphs [0025]-[0027]. In light of such a description in Appellant's application and the generally accepted meaning of the term input/output hub, one skilled in the art simply would not equate a processor card having a general purpose processor with an I/O hub designed to direct I/O traffic between I/O devices.

Furthermore, claims 5 and 6 are similarly structured with claim 5 being directed to memory caching processors and claim 6 being directed to memory caching input/output hubs. The concept of claim differentiation would tend to support the concept that memory caching input/output hubs are not memory caching processors, such as, for example, the processors of the Bealkowski processor cards 11a-11d. For the above reasons, Appellant respectfully requests the rejection of claim 6 be reversed.

Claims 7 and 8

Claim 7 depends from claim 1. Accordingly, claim 7 is allowable for at least the reasons stated above in regard to claim 1. Furthermore. claims 7 and 8 require adding identified ***memory*** of the hot plug module to a memory pool of the running computer system. Again, Bealkowski appears to teach hot-pluggable processor cards. However, the hot-pluggable processor cards do not appear to have any memory. Bealkowski merely indicates that the processors of the processor cards have cache memories. Such cache memories do not increase the storage capacity of the running computer device, but only provide a mechanism for the processors to retain local copies of data stored in the memory 32 of the computer system. As a result, such cache memories are not added to a memory pool of the running computer when the processor card is added to the running computer system.

Page 12 of the Official Action appears to further rely on the service processor 31 of Bealkowski and the service processor 31 and its associated memory for a teaching of the limitations of claims 7 and 8. However, the associated memory of the service processor 31 is not memory of a hot plug module. Nor is there any indication that the

service processor 31 identifies memory of a hot plug module. Furthermore, the associated memory of the service processor 31 is preferably maintained separately from the rest of the computing device as taught by column 5, lines 52-60. Appellant's respectfully fail to see how the service processor 31 and associated memory of Bealkowski having any bearing on the patentability of claims 7 and 8. Appellant's respectfully request the rejection of claims 7 and 8 be withdrawn.

Claims 9 and 10

Each of claims 9 and 10 depends from claim 8. Accordingly, each of claims 9 and 10 is allowable for at least the reasons stated above in regard to claim 8. Furthermore, the reasons stated above for claims 2-4 in regard to requiring both a communication interface of a hot plug module and a communication interface of a running computer system are relevant to the patentability of claim 10. Appellant's respectfully request the rejection of claims 9 and 10 be withdrawn.

Claim 16

Claim 16 requires examining ***a plurality of interface control registers*** in response to a hot plug event, and identifying which of a plurality of hot plug events caused the hot plug interrupt based upon the ***plurality of interface control registers***. As indicated on page 12 of the Official Action, Bealkowski teaches a service processor 31 that has its own associated memory and control routines. Bealkowski further teaches that the service processor 31 monitors events within the data processing system 10. However, Appellant has been unable to locate any teaching in regard to examining ***a plurality of interface control registers*** as required by Appellant's claim

16. Accordingly, Bealkowski does not anticipate claim 16. Appellant respectfully requests the rejection of claim 16 be reversed.

Claims 17-23

Each of claims 17-23 depend from claim 16. Accordingly, each of claims 17-23 is allowable for at least the reasons stated above in regard to claim 16. Further, each of claims 17-23 includes additional novel and nonobvious limitations. For example, claim 17 requires determining whether hot plug addition or hot plug removal has been requested ***based upon an interface control register*** associated with the hot plug module. While Bealkowski discloses hot plug addition and hot plug removal of processors, Bealkowski appears to provide no teaching in regard to determining whether a hot plug addition or a hot plug removal has been requested based upon ***an interface control register*** as required by the invention of Appellant's claim 17. Similarly, Bealkowski appears to provide no teaching in regard to making the determinations of claims 18 and 22 based upon ***an interface control register***. Furthermore, Bealkowski appears to provide no teaching in regard to determining ***that no other hot plug addition is in progress*** as required by claim 23.

Since Bealkowski fails to teach one or more limitations of claims 17-23 as identified above, Bealkowski does not anticipate claims 17-23. Appellant respectfully requests the rejection of claims 17-23 be reversed.

Claims 24-27

Claim 24 requires a hot plug module having a communications interface to establish a communication link with a running computing device in response to being

enabled and to de-establish the communication link in response to being disabled. As stated above in regard to claim 1, Bealkowski does not teach a hot plug module that has a communications interface that can be enabled and disabled. Instead, Bealkowski has switches on the computer system side of a connector to isolate the hot plug module during addition and removal. Furthermore, Bealkowski does not disclose a hot plug module with an interface control register to indicate whether the communication interface is enabled or disabled. Instead, Bealkowski discloses a hot plug control that is on the computer system side of the connector to control FET switches used to isolate the hot plug processor cards.

Each of claims 25-27 depends from claim 24. Accordingly, each of claims 25-27 is allowable for at least the reasons stated above in regard to claim 24. Further, each of claims 25-27 includes additional novel and nonobvious limitations. For example, claim 27 requires that a processor of the hot plug module enable the communication interface of the hot plug module. Bealkowski, however, appears to rely on the hot plug control on the computer system side of the connector to active switches on the computer system side of the connector. There appears to be no teaching of a processor of a hot plug module enabling a communication interface of the hot plug module. Appellant respectfully requests the rejection of claims 24-27 be reversed.

Claims 28-30

Claim 28 requires a midplane having a hot plug interface and a hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device. Bealkowski does not teach a hot plug

module that updates a hot plug interface of a midplane as required by claim 28. As stated above, Bealkowski merely indicates that a service processor and/or a hot plug control of the computer system side of the connector manage FET switches that isolate a processor card during addition and removal. There appears to be no teaching of the processor card updating a hot plug interface on the computer system side of the connector. Since Bealkowski does not teach each and every limitation, Bealkowski does not anticipate claim 28.

Each of claims 29-30 depends from claim 28. Accordingly, each of claims 29-30 is allowable for at least the reasons stated above in regard to claim 28. Further, each of claims 29-30 includes additional novel and nonobvious limitations. For example, claim 30 requires that a hot plug interface detect whether framing packets are received from the hot plug interface. Appellant has reviewed Bealkowski in detail and is unable to locate any teaching of "framing packets". Appellant respectfully requests the rejection of claims 29-30 be reversed.

Claims 31-34

Claim 31 requires a midplane having ***a switch that comprises a plurality of interface control registers***. While Bealkowski teaches FET switches, Bealkowski appears to provide no teaching in regard to a switch ***that has a plurality of interface control registers***. Bealkowski therefore does not anticipate the invention of claim 31 Each of claims 32-34 depends from claim 31. Accordingly, each of claims 32-34 is allowable for at least the reasons stated above in regard to claim 28. Appellant respectfully requests the rejection of claims 31-34 be withdrawn.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

July 6, 2005
Date

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On: July 6, 2005
Signature
Rachael Brown
Date 7/6/05

(viii) Claims appendix.

What is claimed is:

1. (Previously Presented) A method of adding one or more caching agents to a running computing device, comprising

identifying the one or more caching agents provided by a hot plug module in response to the hot plug module being physically coupled to the running computing device;

adding the identified caching agents of the hot plug module to a resource pool of the running computing device; and

enabling a communication interface of the hot plug module to establish a communication link with the running computing device.

2. (Original) The method of claim 1, further comprising

enabling a communication interface of the running computing device that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device.

3. (Previously Presented) The method of claim 2, further comprising

performing a self test of the hot plug module, and

in response to passing the self test, enabling the communication interface of the hot plug module to establish the communication link with the communication interface of the running computing device.

4. (Previously Presented) The method of claim 2, further comprising

initializing the hot plug module, and

after initializing the hot plug module, enabling the communication interface of the hot plug module to establish the communication link with the communication interface of the running computing device.

5. (Original) The method of claim 1 wherein adding comprises adding one or more memory caching processors of the identified caching agents to a processor pool of the running system.

6. (Original) The method of claim 1 wherein adding comprises adding one or more memory caching input/output hubs of the identified caching agents to an input/output pool of the running system.

7. (Original) The method of claim 1 further comprising

identifying memory of the hot plug module in response to the hot plug module being physically coupled to the running computing device; and

adding the identified memory of the hot plug module to a memory pool of the running computing device.

8. (Previously Presented) A method of adding memory to a running computing device, comprising

identifying memory of a hot plug module in response to the hot plug module being physically coupled to the running computing device; and

adding the identified memory of the hot plug module to a memory pool of the running computing device.

9. (Original) The method of claim 8, further comprising

enabling a communication interface of the running computing device that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device.

10. (Previously Presented) The method of claim 8, further comprising

performing a self test of the hot plug module, and

in response to passing the self test, enabling a communication interface of the hot plug module to establish a communication link with the communication interface of the running computing device.

11. (Canceled)

12. (Previously Presented) The method of claim 14, further comprising in response to the hot plug removal request, providing an indication that a hot plug removal is in progress.

13. (Previously Presented) The method of claim 12, further comprising

after removing the identified resources from the running computing device, providing an indication that the hot plug module may be removed.

14. (Previously Presented) A method of removing a hot plug module comprising one or more memory caches from a running computing device, comprising

identifying resources of the hot plug module in response to a hot plug removal request;

causing the hot plug module to write back modified cache lines of the one or more memory caches to the running computing device;

removing the identified resources from respective resource pools of the running computing device;

waiting a predetermined time for pending transactions associated with hot plug module to complete; and

disabling the communication interface of the running computing device to isolate the hot plug module from the running computing device after waiting the predetermined time.

15. (Canceled).

16. (Original) A machine readable medium for interrupt processing, comprising a plurality of instructions that in response to being executed result in a computing device

in response to a hot plug interrupt examining a plurality of interface control registers associated with a plurality of communication interfaces for communicating with a plurality of hot plug modules having caching agents; and

identifying which of a plurality of hot plug events caused the hot plug interrupt based upon the plurality of interface control registers.

17. (Original) The machine readable medium of 16, wherein the plurality of instructions in response to being executed further result in the computing device

determining whether hot plug addition or hot plug removal has been requested for a hot plug module of the plurality of hot plug modules based upon an interface control register of the plurality of interface control registers that is associated with the hot plug module.

18. (Original) The machine readable medium of claim 17, wherein the plurality of instructions in response to being executed further result in the computing device

determining that hot plug removal has been requested for the hot plug module in response to the interface control register associated with the hot plug module indicating a pending hot plug interrupt and a joined state for the hot plug module.

19. (Original) The machine readable medium of claim 18, wherein the plurality of instructions in response to being executed further result in the computing device

causing the hot plug module to write back modified cache lines to the running computing device; and

removing resources of the hot plug module from the computing device.

20. (Original) The machine readable medium of claim 16, wherein the plurality of instructions in response to being executed further result in the computing device

determining that hot plug removal has been requested for the hot plug module;

waiting a predetermined time for pending transactions associated with hot plug module to complete; and

disabling the communication interface of the computing device to isolate the hot plug module from the computing device after waiting the predetermined time.

21. (Original) The machine readable medium of claim 16, wherein the plurality of instructions in response to being executed further result in the computing device

determining that hot plug removal has been requested for the hot plug module; and

disabling the communication interface of the computing device to isolated the hot plug module from the computing device after determining that all transactions associated with the hot plug module have completed.

22. (Original) The machine readable medium of claim 16, wherein the plurality of instructions in response to being executed further result in the computing device

determining that hot plug addition has been requested for the hot plug module in response to the interface control register indicating that the associated communication interface is disabled, that a module is coupled to the associated communication interface, and that the associated communication interface is in a no module present state.

23. (Original) The machine readable medium of claim 22, wherein the plurality of instructions in response to being executed further result in the processor

adding resources of the hot plug module to the running computing device in response to determining that hot plug addition has been requested for the hot plug module and that no other hot plug addition is in progress.

24. (Original) A hot plug module comprising

a coupler for detachably coupling the hot plug module to a running computing device;

a communication interface to establish a communication link with the running computing device via the coupler in response to being enabled and to de-establish the communication link in response to being disabled;

an interface control register associated with the communication interface to indicate and control whether the communication interface is enabled or disabled, and

a processor and associated memory cache, the processor to program the interface control register to enable and disable the communication interface based upon whether the hot plug module is ready to join the running computing device.

25. (Original) The hot plug module of claim 24, wherein

the processor writes back modified cache lines of the memory cache to the running computing device in response to hot plug removal being requested for the hot plug module.

26. (Original) The hot plug module of claim 25, wherein the hot plug module comprises a status indicator that indicates a hot plug status for the hot plug module.

27. (Original) The hot plug module of claim 26, wherein the processor

performs a self test of the hot plug module in response to hot plug addition being requested for the hot plug module, and

enables the communication interface in response to determining that the hot plug module passed the self test.

28. (Original) A computing device comprising,

a midplane comprising a coupler and a hot plug interface to track a state associated with the coupler;

a hot plug module comprising a coupler to detachably couple the hot plug module to the coupler of the midplane and resources coupled to the coupler of the hot plug module via a hot plug interface of the hot plug module, the hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device; and

a processor coupled to the hot plug interface of the midplane, the processor to add the resources to the computing device without rebooting in response to determining that the hot plug interface of the midplane indicates the resources are ready to join.

29. (Original) The computing device of claim 28, wherein

the midplane comprises a hot plug monitor that provides the hot plug interface of the midplane with a signal indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane, and

the processor programs the hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane.

30. (Original) The computing device of claim 28, wherein

the hot plug interface of the midplane detects whether framing packets are received from the hot plug interface of the hot plug module, and

the processor programs the hot plug interface of the midplane to generate a hot plug interrupt in response to a change in receipt of framing packets.

31. (Original) A midplane of a computing device, comprising

a plurality of couplers to detachably couple hot plug modules to the midplane;

at least one switch to interconnect the plurality of couplers, the at least one switch comprising a plurality of communication interfaces to establish communication links with the hot plug modules that are coupled to the plurality of couplers, and a plurality of interface control registers to control the plurality of communication interfaces.

32. (Original) The midplane of claim 31, further comprising

a system management processor to initialize hot plug modules coupled the plurality of couplers.

33. (Original) The midplane of claim 32, wherein the plurality of interface control registers track states of the plurality of communication interfaces and associated hot plug modules.

34. (Original) The midplane of claim 31, wherein the switch provides an indication as to when all pending transactions associated with a hot plug module to be removed have completed.

(ix) Evidence appendix.

None.

(x) Related proceedings appendix.

None.